Amendments to the Specification:

Please replace the paragraph beginning on page 7, line 6 with the following:

Referring now to the drawings wherein the showings are for the purpose of illustrating a preferred embodiment of the invention only and not for purposes of limiting same, Fig. 1 shows a HOST and MAC processor configuration, including a priority-based arbiter 100 in accordance with a preferred embodiment of the present invention. As indicated above, HOST processor [[10]]4 and MAC processor 20 will vie for access to shared bus 60, so as to access shared memory 70. A central memory/bus arbiter 50 determines which processor will be granted access. Host interface 10, MAC processor 20, Central memory/bus arbiter 50, shared bus 60, shared memory 70, and priority-based arbiter 100 reside on a PCI card C1 in accordance with the illustrated embodiment.

Please replace the paragraph beginning on page 8, line 7 with the following:

In accordance with an illustrated embodiment of the present invention, central memory/bus arbiter 50 grants access to shared bus [[70]]60, to either MAC processor 20 or HOST interface 10, giving each equal priority, wherein access is mutually exclusive. Thus, without priority-based arbiter 100 (i.e., priority disabled), when both bus agents (i.e., HOST interface 10 and MAC processor 20) simultaneously request access to shared memory 70, central memory/bus arbiter 50 will grant access to each bus agent on alternating clock cycles ("first come - first serve"). However, with use of priority-based arbiter 100, priority of the bus agent(s) is used to modify access time without modifying central memory/bus arbiter 50, as will be described in further detail below. Central memory/bus arbiter 50 also controls the Data and Address data path and R/W controls out to the shared bus, so data can be transferred between the HOST Interface 10 or MAC processor 20 and the shared memory 70.